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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/964,474	09/28/2001	Takao Ono	H-1012	2772

7590 10/30/2003  
Mattingly, Stanger & Malur, P.C.  
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EXAMINER

CHAMBLISS, ALONZO

ART UNIT PAPER NUMBER

2827

DATE MAILED: 10/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	09/964,474	ONO ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Alonzo Chambliss	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 17 July 2003.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-29 is/are pending in the application.
- 4a) Of the above claim(s) 8-11 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-7 and 12-29 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 September 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☒ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                  | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____  |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                         | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) <u>2</u> . | 6) <input type="checkbox"/> Other: _____                                    |

**DETAILED ACTION**

1. Pre-amendment A filed on 9/28/01 has been fully considered and made of record in Paper No. 3.

***Election/Restrictions***

2. Applicant's election without traverse of claims 1-7 and 12-29 in Paper No. 4 is acknowledged.
3. Claims 8-11 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected claims, there being no allowable generic or linking claim.

***Priority***

4. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Japan on 10/5/00. It is noted, however, that applicant has not filed a certified copy of the JP 2000-305633 application as required by 35 U.S.C. 119(b).

***Information Disclosure Statement***

5. The information disclosure statement (IDS) submitted on 9/28/01 in Paper No. 2 was filed before the mailing date of the non-final rejection on 10/19/03. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

***Drawings***

6. Figures 12, 13, 14a, and 14b should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

***Specification***

7. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The following title is suggested: MEMORY SYSTEM WITH A SOCKET HAVING SOCKET PINS FOR MOUNTING MEMORY MODULES ”.

***Claim Rejections - 35 USC § 112***

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 26 and 28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

10. Claims 26 and 28 recite the limitation " said connecting member " in line 2. There is insufficient antecedent basis for this limitation in the claim.

***Claim Rejections - 35 USC § 103***

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

12. Claims 1, 4, 5, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakase et al. (U.S. 6,392,897) in view of Koichiro (JP 1-3971).

With respect to Claims 1, 4, and 5 Nakase discloses a socket 14(i.e. the area around the socket pins 15a, 15b) having a plurality of socket pins 15a, 15b branched from one point, wherein the wirings 11 on the mother board 9 are connected to each of the plurality of memory modules 1a by using the socket 14. The memory controller 10 is connected to each of the plurality of memory modules 1a (see col. 10 lines 1-22; Fig. 2). Nakase fails to explicitly disclose wherein the memory controller is connected to each of the plurality of memory modules in an equal distance. However, Koichiro

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discloses a plurality of modules 1 electrically connected to plurality socket pins 2, which are electrically connected to the main printed circuit board by a single terminal post 6 (see English translation, paragraphs 4-10; Fig. 3). Thus, the wirings 11 of Nakase are electrically connect to terminal post 6 (i.e. one point) on the top surface of the main printed circuit board which is connected to the socket pins 2 in Koichiro. Nakase and Koichiro have substantially the same environment of a plurality of memory modules connected to a motherboard by a socket with socket pins. Therefore, it would have been obvious to substitute the socket arrangement with a single terminal post for the socket arrangement of Nakase, since the socket arrangement would provide a faster signal path between a controller and a plurality of memory modules as taught by Koichiro.

With respect to Claim 7, Nakase discloses wherein termination resistors 112 are connected to one ends of the plurality of wirings 111 (see col. 2 lines 24-29; Fig. 18).

### ***Claim Rejections - 35 USC § 102***

13. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

14. Claim 12-16, 19, 21, and 24-29 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Nakase et al. (U.S. 6,392,897).

With respect to Claims 12 and 24, Nakase teaches a memory control device 10 laid out on the board 9, including a first terminal (i.e. leads extending from the controller), a connecting member 14 laid out on the board 9, which includes a first mounting part having a second terminal and a second mounting part having a third terminal corresponding to the second terminal, wherein a first memory module 1a can be mounted on the first mounting part, wherein a second memory module 1a can be mounted on the second mounting part, wherein the first memory module 1a has a fourth terminal 4a, wherein the second memory module has a fifth terminal 4a, wherein, when the first memory module is mounted on the first mounting part, the second terminal is connected to the fourth terminal, wherein when the second memory module 1a is mounted on the second mounting part, the third terminal is connected to the fifth terminal 4a, and wherein the shortest distance of wirings between the first terminal of the control device 10 and the second terminal of the first mounting part is substantially equal (i.e. close to but not equal to) to the shortest distance of wirings 11 between the first terminal of the control device 10 and the third terminal of the second mounting part. (see col. 10 lines 1-40 and col. 11 lines 23-43; Figs. 1-18).

With respect to Claim 13, Nakase teaches wherein both the second terminal and third terminal is a data terminal (i.e. for data signals) (see col. 2 lines 40-46).

With respect to Claim 14, Nakase teaches wherein the connecting member 14 comprises a sixth terminal, wherein the board 9 further comprises a first board wiring

that connects the first terminal with the sixth terminal, and wherein the connecting member 11 further comprises a first wiring member 15a connected between the sixth terminal and the second terminal, and a second wiring member 15c connected between the sixth terminal and the third terminal (see Figs. 1-18).

With respect to Claim 15, Nakase teaches wherein a length of the first wiring member 15a is substantially equal (i.e. close to but not equal to) to a length of the second wiring member 15c (see Figs. 1-18).

With respect to Claims 16 and 27, Nakase teaches wherein the connecting member is a socket 14, wherein the first mounting part and the first wiring member constitute a first socket pin 15a, and wherein the second mounting part and the second wiring member constitute a second socket pin 15c (see Figs. 1-18).

With respect to Claim 19, Nakase teaches more than eleven terminal represent by 4a and 4b on each module 1a in Fig. 1 which are electrically connected to socket pins 15a, 15c that connect to controller 10 in Figs. 1-18. Therefore, the first memory module 1a further comprises a sixth terminal, wherein the second memory module 1a comprises a seventh terminal corresponding to the sixth terminal, wherein the first mounting part further comprises an eighth terminal, wherein the second mounting part further comprises a ninth terminal, wherein, when the first memory module 1a is mounted on the first mounting part, the sixth terminal is connected to the eighth terminal, wherein when the second memory module 1a is mounted on the second mounting part, the seventh terminal is connected to the ninth terminal, and wherein the

control device further comprises a tenth terminal connected to the eighth terminal and an eleventh terminal connected to the ninth terminal (see col. 10 lines 1-50; Figs. 1-18).

With respect to claim 21, Nakase teaches wherein the eighth terminal is a terminal to receive a first chip selecting signal and wherein the ninth terminal is a terminal to receive a second chip selecting signal (see col. 10 lines 41-65 and col. 11 lines 13-67; Figs. 1-18).

With respect to Claim 25, Nakase teaches more than eleven terminal represent by 4a and 4b on each module 1a in Fig. 1 which are electrically connected to socket pins 15a, 15c that connect to controller 10 in Figs. 1-18. Therefore, a first mounting part 15a, 15c having a first terminal, a second mounting part 15a, 15c having a second terminal corresponding to the first terminal, and a third terminal, wherein a first memory module 1a can be mounted on the first mounting part 15a, 15c wherein a second memory module 1a can be mounted on the second mounting part 15a, 15c, wherein the first memory module 1a has a fourth terminal, wherein the second memory module 1a has a fifth terminal corresponding to the fourth terminal, wherein when the first memory module 1a is mounted on the first mounting part 15, 15c, the first terminal is connected to the fourth terminal, wherein the second memory module 1a is mounted on 1a second mounting part 15a, 15c the second terminal is connected to the fifth terminal, wherein the third terminal is connected to the first terminal of the first mounting part 15a, 15c by a first wiring member, wherein the third terminal is connected to the second terminal of the second mounting part 15a, 15c by a second wiring member, and wherein a length of

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the first wiring member is equal to a length of the second wiring member (see col. 10 lines 1-40 and col. 11 lines 23-43; Figs. 1-18).

With respect to Claims 26 and 28, Nakase teaches wherein the connecting member 14 is a memory module socket that is laid on a mounting board 9 (see Figs. 1-18).

With respect to Claim 29, Nakase teaches wherein both the first terminal and the second terminal are a data terminal (see col. 10 lines 24-40).

15. Claims 2, 3, 17, 18, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakase et al. (U.S. 6,392,897) and Koichiro (JP 1-3971) as applied to claims 1 and 12 above, and further in view of Billman et al. (4,756,694) and Sanwo et al. (U.S. 5,530,623).

With respect to Claims 2 and 17, Nakase-Koichiro both fail to disclose wherein each of the plurality of memory modules is mounted in a radial form on the motherboard by way of the plurality of socket pins of the socket. However, Billman discloses wherein each of the plurality of memory modules "D" is mounted in a radial form on the motherboard "M" by way of the plurality of socket pins 18 of the socket "H" (see Figs. 5 and 6). Nakase-Koichiro and Billman have substantially the same environment of a plurality of memory modules mounted on a printed circuit board. Therefore, it would have been obvious to substitute the radial arrangement for the perpendicular arrangement of Nakase-Koichiro, since the radial arrangement would provide a low profile package as taught by Billman.

With respect to Claims 3 and 18, one skilled in the art at the time of invention would readily recognize bending the socket pins 18 so that the plurality of memory modules can be mounted in parallel to the mother board by way of the plurality of socket pins 18 of the socket " H ", since the bending of the socket pins allowing the memory modules to be parallel the mother board would provide an even lower profile package than the radial arrangement. Therefore, it would have been obvious to incorporate a parallel arrangement of memory modules, since the bending of the socket pins allowing the memory modules to be parallel the motherboard would provide an even lower profile package than the radial arrangement.

With respect to Claim 23, it is well known it to attach a plurality of dynamic memory chips to first and second memory modules as evident by Sanwo (see col. 1 lines 18-30).

16. Claims 6, 20, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakase et al. (U.S. 6,392,897) and Koichiro (JP 1-3971) as applied to claims 1 and above, and further in view of Leung et al. (U.S. 5,592,632).

With respect to Claims 6, 20, and 22, it is well known in the semiconductor industry to have plurality of socket pins in a socket where the pins are for an address signal, a control signal, a data signal, and a data management signal are common to each of the plurality of memory modules, the pins for a clock signal, a clock management signal, a bank selecting signal, and a power supply signal are separated with each of the plurality of memory modules as evident by Leung (see col. 11 lines 62-67 and col. 12 lines 1-67, and col. 13 lines 1-67; Figs. 1-9). Thus, allowing Nakase to

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have a eighth terminal that is a terminal to receive a first clock enable signal and a ninth terminal that is a terminal to receive a second clock enable signal.


The prior art made of record and not relied upon is cited primarily to show the product of the instant invention.

### ***Conclusion***

17. Any inquiry concerning the communication or earlier communications from the examiner should be directed to Alonzo Chambliss whose telephone number is (703) 306-9143. The fax phone number for this Group is (703) 308-7722 or 7724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-7956

**AC**/October 20, 2003

  
Alonzo Chambliss  
Patent Examiner  
Art Unit 2827